AMENDMENTS TO THE CLAIMS

1. (previously presented) A flash memory device comprising:

an array of non-volatile memory cells;

a clock signal connection to receive a clock signal comprising clock cycles;

a rambus dynamic random access memory (RDRAM) interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections;

sense amplifier circuitry coupled to the memory cells over bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell; and

command logic coupled to the array to provide two data access operations per clock cycle, wherein the command logic includes control registers used to store data for memory operation control.

2. (previously presented) The flash memory device of claim 1, wherein the array of non-volatile memory cells is arranged in a plurality of addressable banks.

3. (previously presented) The flash memory device of claim 2 wherein each addressable bank contains addressable sectors of memory cells.

4. (previously presented) The flash memory device of claim 1, wherein the data connections are burst oriented and the command logic comprises means for starting data access at a selected location and continuing for a programmed number of locations in a programmed sequence

5. (previously presented) The flash memory device of claim 1, wherein the pre-charge circuitry pre-charges an active digit line that is coupled to read a memory cell to a voltage that is greater than a complementary digit line.

6. (previously presented) The flash memory device of claim 1, wherein the pre-charge circuitry pre-charges the bit lines to a differential level using charge sharing.

7. (previously presented) The flash memory device of claim 1, wherein the pre-charge circuitry pre-charges the bit lines to a differential level using a bias circuit.

8. (previously presented) A processing system comprising:

a processor; and

a rambus dynamic random access memory compatible flash memory device coupled to the processor, the memory device comprising:

an array of non-volatile memory cells;

a clock signal connection to receive a clock signal comprising clock cycles;

a rambus dynamic random access memory interconnect configuration coupled to the array of non-volatile memory cells, the interconnect configuration comprising a multiplexed row address bus, a multiplexed column address bus, and data connections that are burst oriented;

sense amplifier circuitry coupled to the memory cells over bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell; and

command logic coupled to the array to provide two data access operations per clock cycle starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

9. (previously presented) The system of claim 8, wherein the processor generates flash memory compatible control signals.

10. (previously presented) The system of claim 8, wherein the processor is adapted to receive burst transmissions of data from the memory device.

11. (previously presented) The system of claim 8, wherein the non-volatile memory device is a flash memory device.

12. (previously presented) A processing system comprising:

a processor;

a single communication bus coupled to the processor;

a volatile memory device coupled to the single communication bus; and

a rambus dynamic random access memory (RDRAM) compatible flash memory device comprising:

an array of non-volatile memory cells;

a clock signal connection to receive a clock signal comprising clock cycles;

sense amplifier circuitry coupled to the memory cells over bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines;

pre-charge circuitry coupled to pre-charge the bit lines to first and second voltage levels to provide an initial differential voltage prior to sensing a memory cell; and

command logic coupled to the array of non-volatile memory cells to provide two data access operations per clock cycle following an RDRAM compatible format and starting at a selected location and continuing for a programmed number of locations in a programmed sequence.

13. (previously presented) The processing system of claim 12, wherein the volatile memory device and the RDRAM compatible flash memory device both respond to common command signals provided on the single communication bus.

14. (currently amended) The processing system of claim 12, wherein the two data access operations per clock cycle are performed on clock transitions ~~transistions~~.

15. (previously presented) The processing system of claim 12, wherein the memory cells are floating gate memory cells.

16. (previously presented) The processing system of claim 12, wherein the processor generates computer system commands.